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2013 Nanotechnology 24 505718

(http://iopscience.iop.org/0957-4484/24/50/505718)

Nanotechnology **24** (2013) 505718 (8pp) doi:10.1088/0957-4484/24/50/505718

Significant reduction of thermal conductivity in silicon nanowire arrays

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Received 2 August 2013, in final form 18 October 2013
Published 27 November 2013
Online at stacks.iop.org/Nano/24/505718

Abstract
Vertically aligned single-crystal silicon nanowire arrays (SiNWs) with various lengths, surface roughnesses and porosities were fabricated with the metal-assisted chemical etching method. Using the laser flash technique and differential scanning calorimetry, we characterized the thermal conductivities of bulk SiNWs/Si/SiNWs sandwich-structured composites (SSCs) at room temperature (300 K). The results demonstrate that the thermal conductivities of SSCs notably decrease with increases in the length, surface roughness and porosity of SiNWs. Furthermore, based on the series thermal-resistance model, we calculated the thermal conductivity of porous SiNWs to be as low as 1.68 W m^{-1} K^{-1} at 300 K. Considering the remarkable phonon scattering from the diameter, surface roughness and porosity of SiNWs, leading to a significant reduction of the thermal conductivity, SSCs and SiNWs could be applied to high-performance thermoelectric devices.

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon has been extensively used in the optoelectronic and microelectronic fields for many years, but not in the thermoelectric field because of its high thermal conductivity (142 W m^{-1} K^{-1} at 300 K for bulk intrinsic silicon [1, 2]). In the last decade, reports about the thermal conductivities of silicon nanostructures have obviously increased [3–19]. Phonon scattering at the nanometer scale, particularly at scales smaller than the bulk phonon mean free path ($\Lambda \sim$ 300 nm at 300 K for silicon [20, 21]), can be strongly enhanced owing to various scattering mechanisms, such as phonon-boundary scattering, phonon-impurity scattering and phonon-interface scattering, so the thermal conductivities of silicon nanostructures are reduced by two or three orders of magnitude compared with that of bulk silicon. For instance, the thermal conductivity of nanostructured bulk silicon is 6.3 W m^{-1} K^{-1} at room temperature [4], and the thermal conductivity for phosphorus-doped (2.3×10^{20} cm^{-3}) silicon layers of 30 nm thickness is reduced to 12 W m^{-1} K^{-1} at 300 K [5].

Among these silicon nanostructures, silicon nanowires have attracted considerable attention in recent works [9–19]. Boukai *et al* reported that 10 nm wide silicon nanowires exhibit extremely low thermal conductivity (0.76 W m^{-1} K^{-1} at 300 K) [16]. The Hochbaum group reported that when silicon nanowire has a rough or porous surface, even at 52 nm in diameter, it still has a low thermal conductivity (1.6 W m^{-1} K^{-1} at room temperature) that is comparable with that of insulating glass [14]. That is, all reports have indicated that forming silicon into nanowires can reduce its thermal conductivity to a low level, and these nanowires are very promising for application in thermoelectric devices. Therefore, it is worthwhile to study the thermal conductivities of large-area silicon nanowire arrays (k_{SiNWs}) with varying diameters, surface roughnesses

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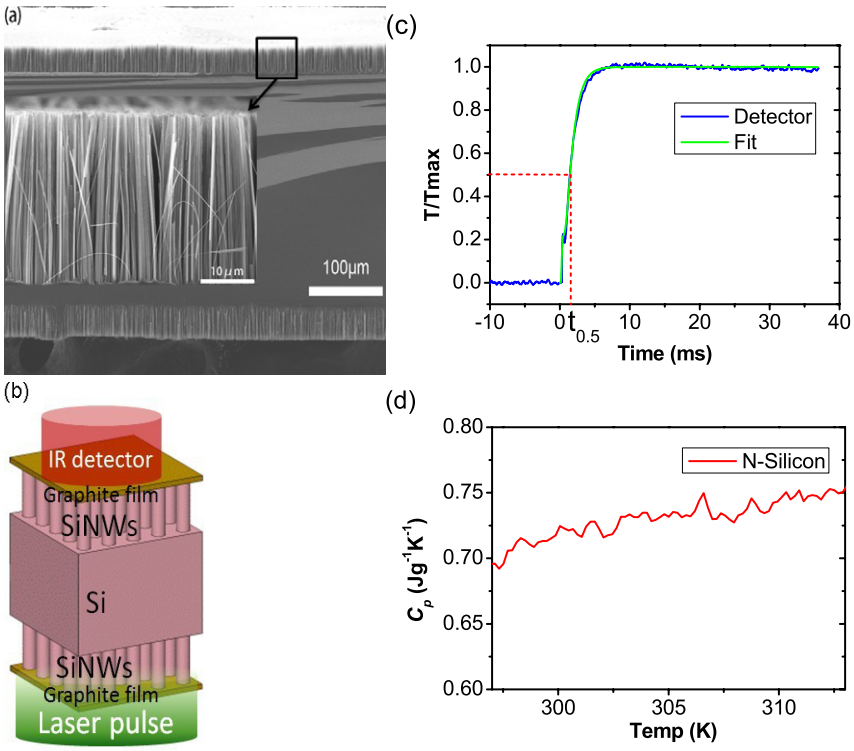

Figure 1. (a) A typical SEM image of the SSCs on p-type silicon prepared with a 180 min etching time. (b) Schematic of the measurement principle for the thermal diffusivity of SSCs using the laser flash method. (c) The characteristic thermogram for the flash method implemented on n-type SSCs prepared with a 240 min etching time. (d) The specific heat capacities of n-type silicon as a function of temperature as measured by differential scanning calorimetry.

and porosities. Although some investigations have been conducted regarding k_{SiNWs}, the SiNWs usually were of uniform diameter [22] or had been embedded in other materials to form nanocomposites [23]. However, there have been few investigations of the thermal conductivity of smooth or porous SiNWs of heterogeneous diameters without filling components. In this work, we fabricated vertically aligned single-crystal SiNWs including wires of diverse lengths, surface roughnesses and porosities with diameters from 20 to 200 nm using the metal-assisted chemical etching method, and we studied the thermal conductivities of the bulk SiNWs/Si/SiNWs sandwich-structured composites (SSCs) at 300 K with the laser flash technique and differential scanning calorimetry. The k_{SiNWs} were determined and discussed by the series thermal-resistance model. It is found that the morphologies of SiNWs can significantly affect the thermal conductivities of SiNWs and bulk SSCs.

2. Experiment methods

The metal-assisted chemical etching method has been widely used for synthesizing large-area SiNWs because of its simple process and good controllability [24–26]. As we have reported previously [27], the length and surface characteristics of SiNWs can be controlled by adjusting the etching conditions and using various silicon substrates with different doping levels. Herein, SiNWs were prepared on lightly phosphorus-doped (n-type, 4×10^{15} cm^{-3}) and highly boron-doped (p-type, 2×10^{19} cm^{-3}) silicon wafers with a (100) crystal orientation and a 10×10 mm^2 area. By etching two sides of the silicon wafers, we obtained bulk SiNWs/Si/SiNWs sandwich-structured composites (SSCs). Specifically, the silicon wafers were first washed ultrasonically in deionized water, acetone and ethanol in succession for 10 min each and then boiled in a solution of H_2SO_4 and H_2O_2 with a volume ratio of 4:1 for 20 min. After the standard cleaning steps, the wafers were immersed in a solution of 0.01 M $AgNO_3$ and 4.8 M HF for 1 min to deposit Ag nanoparticles and then rapidly transferred into a solution of 0.2 M H_2O_2 and 4.8 M HF for the chemical etching. Samples were prepared with various etching times of 30, 60, 120, 180 and 240 min. At the end of the etching process, the etched samples were dipped in a 50% HNO_3 solution to dissolve the Ag residues and then dried naturally in air. The morphologies of SSCs and SiNWs were characterized by a field-emission scanning electron microscope (SEM) (Hitachi S-4800, Japan) and a high-resolution transmission electron microscope (TEM) (JEOL JEM-2010, Japan). Figure 1(a) shows a typical SSC morphology.

In heat-transfer analysis, the thermal conductivity (k) is calculated from the thermal diffusivity (α), the specific heat capacity (C_p) and the mass density (ρ) according to the following formula:

$$k(T) = \alpha(T)\rho(T)C_p(T). \quad (1)$$

The thermal diffusivities of the SSCs were measured using the laser flash method [28] (NETZSCH LFA-457, Germany),

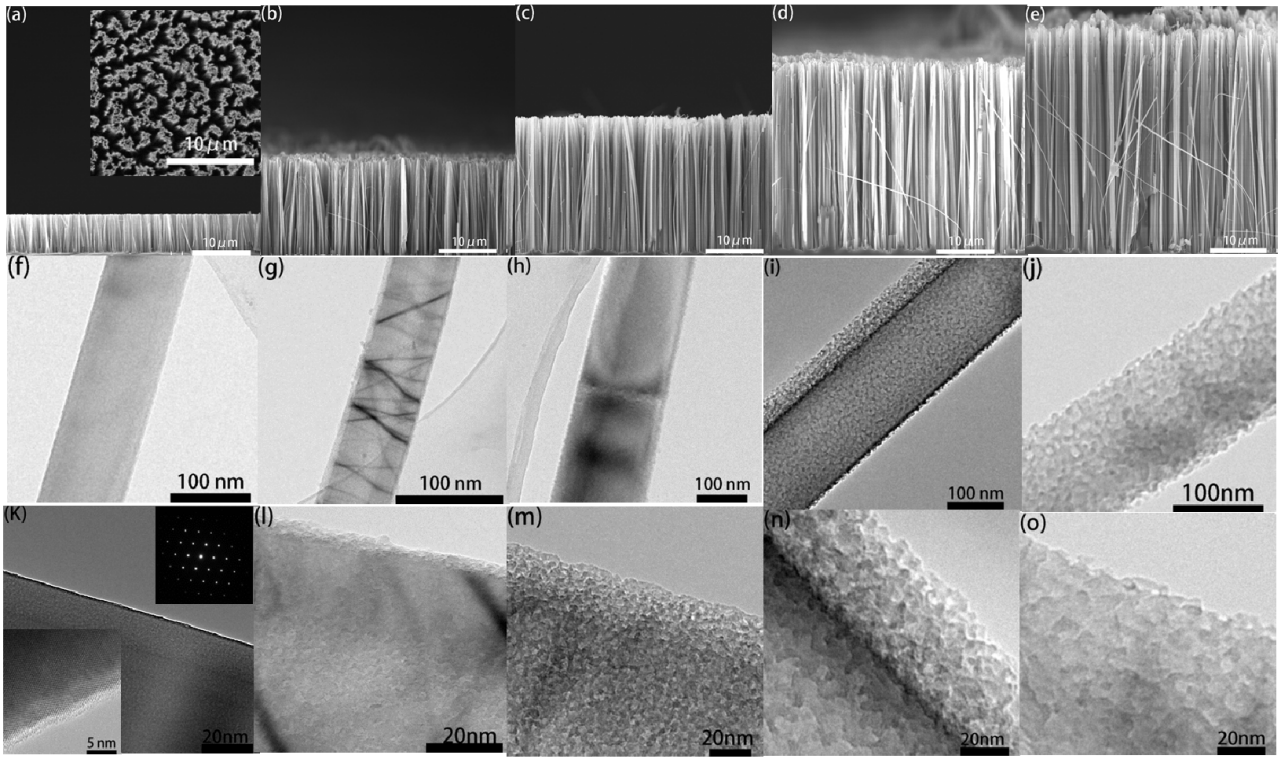

Figure 2. SEM and TEM images of the variable morphology of SiNWs obtained from n-type silicon wafers, with the etching times of 30 min ((a), (f), (k)), 60 min ((b), (g), (l)), 120 min ((c), (h), (m)), 180 min ((d), (i), (n)), and 240 min ((e), (j), (o)). The inset in (a) is the corresponding top-view SEM image, and the insets in (k) are the corresponding SAD pattern and high-resolution images.

and the measurement schematic is illustrated in figure 1(b). To modify the energy absorption and infrared emissivity of the SSCs, a thin film of graphite powder is sprayed on two sides of the sample before testing. When the temperature of the sample reaches 300 K in the furnace, a burst of energy emanating from a short laser pulse acts on one face of the sample and is absorbed, resulting in homogeneous heating. The absorbed heat propagates through the sample and causes a temperature increase on the other surface. This temperature rise is measured versus time using an infrared detector. By fitting the data with finite-pulse and heat-loss corrections [29], the thermal diffusivity of the SSCs is calculated from the specimen thickness and the time ($t_{0.5}$), which is the time required for the temperature to rise from 300 K to half of its maximum value (as seen in figure 1(c)).

The specific heat capacities of the SSCs were determined with the 'three-step' method using differential scanning calorimetry (Seiko SII DSC 6220, Japan), similar to other reports [30, 31]. Briefly, when the SSC sample is heated from 290 to 300 K at a rate of 2 K min^{-1}, the heat flow rate into the sample is proportional to the sample's instantaneous specific heat. By recording this heat flow rate as a function of temperature and comparing it with the heat flow rates into a sapphire standard sample and an empty sample pan under the same conditions, the specific heat of the sample can be determined as a function of temperature (figure 1(d)). Lastly, the mass densities of the SSCs were calculated from their spatial volume and mass, that were measured by an electronic balance (Shimadzu BL-220H, Japan).

3. Results and discussion

3.1. The morphology of the SiNWs

The formation mechanism of the SiNWs is similar to those reported in previous studies [32–34]. As the catalyst, Ag nanoparticles are first deposited via Ag^+ reduction in the $AgNO_3$/HF solution and then oxidized into Ag^+ ions by H_2O_2. The Ag^+ ions acquire electrons from the surrounding silicon and are deoxidized into Ag nanoparticles again. The surrounding silicon is oxidized and dissolved in the H_2O_2/HF solution, resulting in the etching of the silicon surface and the formation of the SiNWs. More importantly, during the etching process, the bottom Ag^+ ions can diffuse upward because there is a lower concentration of Ag^+ ions, and they can be recovered into Ag nanoparticles on the sidewalls of the silicon nanowires where there are defective sites. For highly doped wafers, the dopants can supply many defective sites on the nanowires, which serve as the nucleation centers for Ag nanoparticles and the etching points for the formation of porous SiNWs; in contrast, lightly doped wafers with only a few dopant sites are likely to form rough or even smooth SiNWs because of the relative lack of defective points on the nanowires for Ag-nanoparticle nucleation.

Figure 2 shows the variable morphology of the SiNWs obtained from lightly doped n-type silicon wafers with different etching times. From the SEM images, we observe that the vertically aligned SiNWs distribute uniformly across the entire substrate with diameters from 20 to 200 nm (see

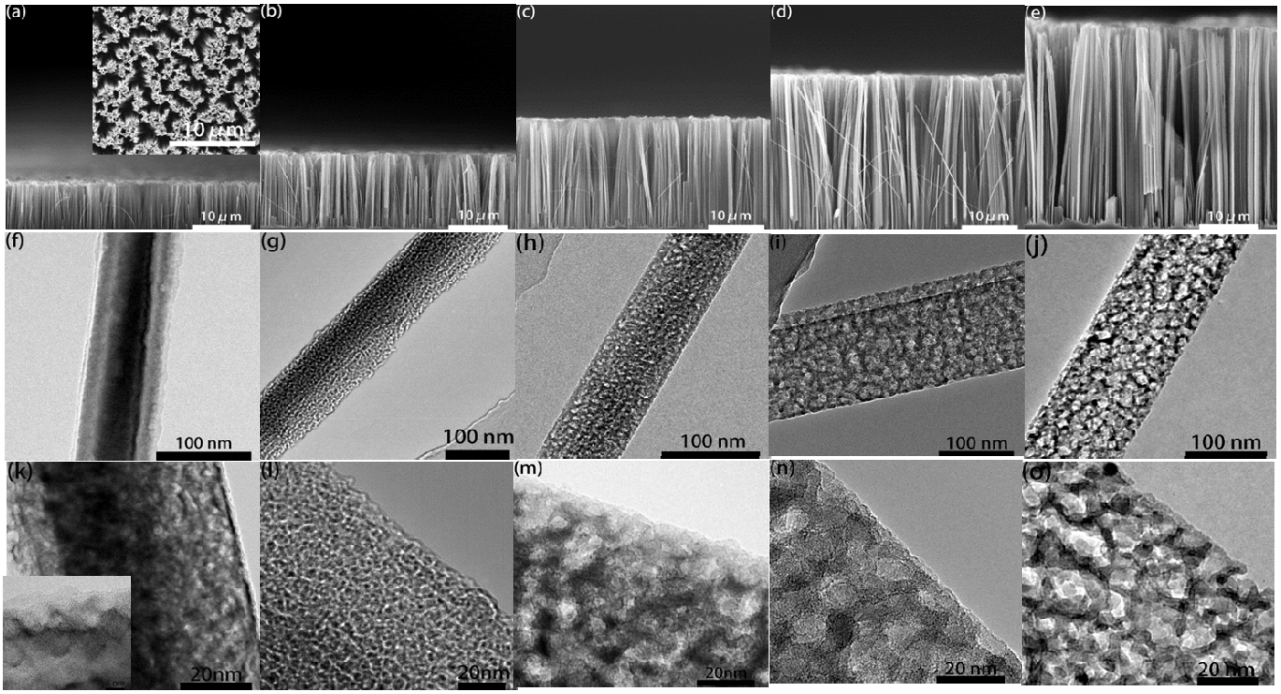

Figure 3. SEM and TEM images of the variable morphology of the SiNWs obtained from p-type silicon wafers, with the etching times of 30 min ((a), (f), (k)), 60 min ((b), (g), (l)), 120 min ((c), (h), (m)), 180 min ((d), (i), (n)), and 240 min ((e), (j), (o)). The inset in (a) is the corresponding top-view SEM image and the inset in (k) is the corresponding high-resolution image.

appendix figure A.1) and with their tips bundled together with interspaces of several micrometers between the bundles, as can be seen from the top-view inset in figure 2(a). As the etching time is extended from 30 to 240 min, the length of the SiNWs increases from 7.16 to 43.27 μm, yet the interspaces of the tip bundles are not enlarged. A few one-dimensional sheet and pillar nanostructures are also formed by several individual silicon nanowires congregating together, especially in the SiNWs prepared with longer etching times. The TEM images indicate that the surfaces of the individual silicon nanowires clearly change from smooth to rough as the etching time is extended from 30 to 240 min. When etched for 30 min, the silicon nanowire is smooth, and no defect with a ⟨100⟩ lattice orientation can be seen from the SAD pattern or high-resolution images, shown as insets in figure 2(k). However, when etched for 60 min, the silicon nanowire appears to have a slightly rough surface, and the roughness increases rapidly as the etching time increases up to 180 min, indicating that the diameter and the depth of the nanopores increase with etching time. Beyond 180 min, the roughness of the silicon nanowire increases slowly, showing little difference between the silicon nanowires etched for 180 and 240 min. This could be attributed to the sharp concentration reduction of the H_2O_2/HF etching solution with longer etching time.

The morphology of the SiNWs etched on highly doped p-type silicon wafers with varying etching times is presented in figure 3. As in the case of the n-type SiNWs (N-SiNWs), the length of the p-type SiNWs (P-SiNWs) also increases as the etching time is extended; however, for the porous P-SiNWs, the longer etching time would cause the tips of the silicon nanowires to cluster together more easily to support themselves, and the interspaces of the tip bundles are enlarged. Table 1 lists the effects of the etching time on some parameters, including the fill-factor (FF) of silicon nanowires within the SiNWs, the average diameters of the nanopores (PD_{ave}) on p-type SiNWs, and the length of a SiNWs which is the total length of the two sides of the SiNWs. From these data, we can see that the vertical etching rates of the two types of SiNWs are different. Generally, P-SiNWs have a slower vertical etching rate than N-SiNWs. According to the described formation mechanism, the Ag^+ ions at the roots of the silicon nanowires can diffuse out and renucleate near the defective sites on the nanowire sidewalls. Thus, for highly doped P-SiNWs, the more Ag nanoparticles nucleate on the sidewall, the less Ag is left at the nanowire roots, which generates a slower etching rate in the vertical direction and a more severe etching on the nanowire sidewalls. This effect is also demonstrated by the TEM images in figure 3. Consistent with the above discussion, a higher degree of porosity is observed in the P-SiNWs, and it is amplified as the etching time increases. Moreover, it is found that the nanopores on P-SiNWs seem to be larger than those on N-SiNWs prepared with the same etching time, and this trend is particularly evident in the case of nanowires prepared with longer etching times. This effect is mainly explained by the fact that the new Ag nanoparticles nucleate around the defects of the wires, some nucleation centers exist near the formed nanopores, and the newly etched nanopores overlap with the original ones [34]. The overlap of the nanopores occurs only in highly doped SiNWs, which is another reason for the formation of porous, rather than rough, SiNWs on highly doped silicon

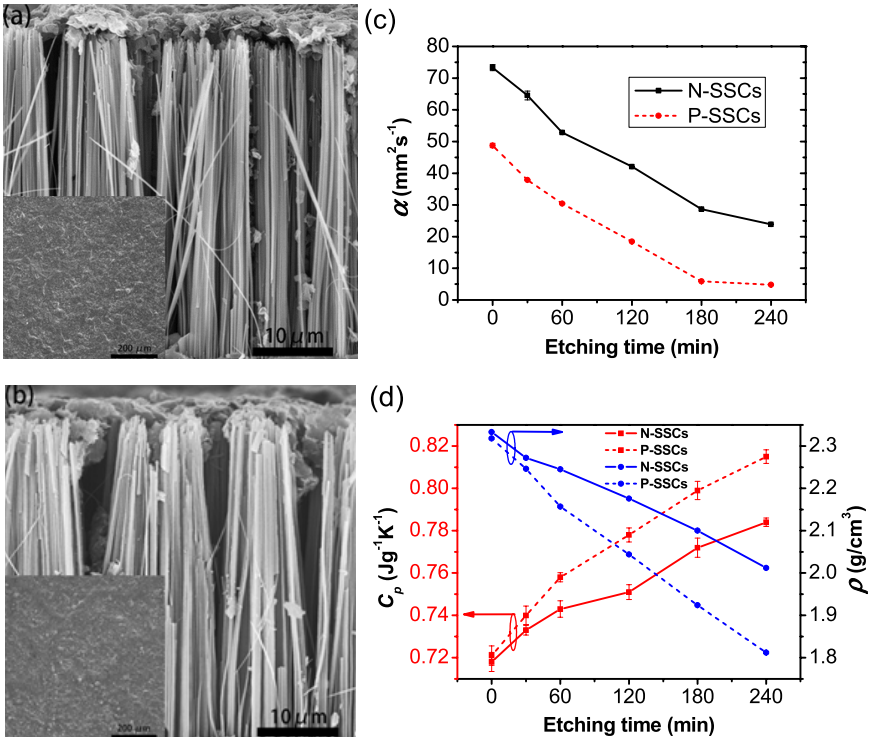

Figure 4. The thermal properties of n-type and p-type SSCs etched for different times. The SEM images of (a) and (b) exhibit the sprayed graphite film on the N-SiNWs and P-SiNWs prepared with an etching time of 240 min. The insets in (a) and (b) are the corresponding top-view SEM images. (c) and (d) show the thermal diffusivity (α), the specific heat capacity (C_p) and the mass density (ρ) of the different type of SSCs as a function of the etching time. All data are measured at 300 K.

Table 1. A list of some parameters of SiNWs and SSCs etched for varying times. (Note: the etching time of 0 min denotes silicon wafers without SiNWs; the length of a SiNWs is the total length of the two sides of the SiNWs; FF and PD_{ave} represent the fill-factor of silicon nanowires within the SiNWs and the average diameters of the nanopores on p-type silicon nanowires respectively.)

		Etching time (min)					
		0	30	60	120	180	240
Length (μm)	N-SiNWs	0	14.33	36.37	50.43	70.17	86.54
	N-SSCs	522.9	523.8	521.1	519.4	518.9	516.8
	P-SiNWs	0	19.80	30.29	45.69	64.23	81.26
	P-SSCs	388.3	387.4	380.1	376.8	379.5	369.8
FF	N-SiNWs	0	0.736	0.731	0.729	0.722	0.719
	P-SiNWs	0	0.723	0.680	0.672	0.659	0.656
PD_{ave} (nm)	P-SiNWs	0	3.52 ± 0.27	5.25 ± 0.59	7.62 ± 1.48	11.14 ± 1.05	13.61 ± 0.99

wafers. Similar to the N-SiNWs, the degree of porosity of the P-SiNWs exhibits little variation as the etching time is increased from 180 to 240 min because of the concentration reduction of the etching solution.

3.2. The thermal conductivity of the SSCs

Figures 4(a) and (b) display the graphite film sprayed onto the N-SiNWs and P-SiNWs prepared with an etching time of 240 min. As previously mentioned, the SiNWs etched for 240 min possess the largest interspaces of bundles in our samples. However, the interspaces are not stuffed with the graphite powder, though some small flakes sink into them. This may be caused by the weak fluidity and quick solidification of fast-spraying graphite powder. The graphite films have a thickness of 2–4 μm and completely cover the top surfaces of the wafer-scale SiNWs, as seen from the top-view SEM images inset in figures 4(a) and (b). From figure 4(c), we can observe that the thermal diffusivities of the two types of SSCs decrease as the etching time increases, which demonstrates that the morphology of the SiNWs, including length, roughness and porosity, has significant influence on the thermal diffusivity of the SSCs. Normally, the longer, rougher and more porous the SiNWs are, the lower the thermal diffusivity of the SSCs is. In addition, the mass densities of the two types of SSCs also decline with the extension of the etching time, and those of the P-SSCs decrease more rapidly (figure 4(d)). This could be attributed to the greater air fraction originating from the larger interspaces of bundles in the P-SSCs, especially for longer etching times. In

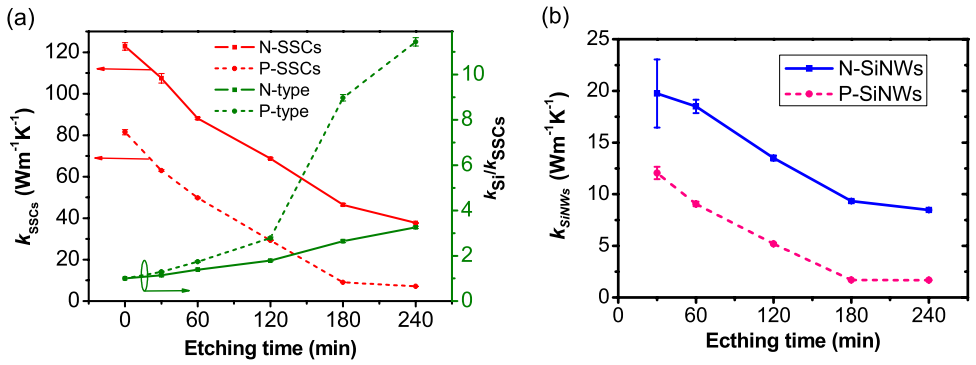

Figure 5. (a) The thermal conductivity (k_{SSCs}) of the different types of SSCs, and (b) the thermal conductivity of silicon nanowire arrays (k_{SiNWs}) as a function of the etching time at 300 K. The values of k_{Si}/k_{SSCs} are given in (a), as well.

contrast, the specific heat capacities of the two types of SSCs increase as the etching time increases, but not remarkably, and the specific heat capacities of the P-SSCs are higher than those of the N-SSCs prepared with the same etching times (figure 4(d)). Although the greater air fraction may account for this phenomenon, the larger specific surface area and phonon-confinement effect of the SiNWs could also cause the specific heat capacity of the SSCs to rise [35]. From equation (1), we acquired the thermal conductivities of the two types of SSCs at 300 K as a function of the etching time, shown in figure 5(a), and the error of k_{SSCs} is obtained from the following equation (2):

$$\Delta k = \sqrt{\left(\frac{\partial k}{\partial \alpha}\Delta\alpha\right)^2 + \left(\frac{\partial k}{\partial C_p}\Delta C_p\right)^2 + \left(\frac{\partial k}{\partial \rho}\Delta\rho\right)^2}. \quad (2)$$

Here, $\Delta\alpha$, ΔC_p and $\Delta\rho$ are the measurement errors of the thermal diffusivity, the specific heat capacity and the density of the SSCs, respectively, at 300 K. The results reveal that the thermal conductivities of the lightly doped n-type and highly doped p-type single-crystal bulk silicon wafers are 122.82 and 81.47 W m^{-1} K^{-1} at 300 K, respectively, which is the result of the enhancement of the phonon-impurity scattering effect in the highly doped silicon wafer. The data are quite similar to those of previous works [2–4] that reported the thermal conductivities of phosphorus-doped (n-type, 2×10^{19} cm^{-3}) and boron-doped (p-type, 1×10^{20} cm^{-3}) bulk silicon are approximately 110 and 80 W m^{-1} K^{-1} at 300 K, respectively. Additionally, the k_{SSCs} values of the n-type and p-type wafers decrease linearly as the length, roughness or porosity of the SiNWs increase as a result of increased etching time. When the sample is etched for 240 min, the k_{SSCs} of the n-type sample is 37.69 W m^{-1} K^{-1} and 3.26 times lower than that of the corresponding bulk silicon at 300 K, while that of the p-type sample is 7.12 W m^{-1} K^{-1} and 11.44 times lower than that of its bulk silicon counterpart at room temperature. It is expected that we could attain a very low thermal conductivity of the SSCs through increasing the length, roughness and porosity of the SiNWs while not changing the fill-factor of SiNWs which is crucial to achieve excellent thermoelectric performance [36].

3.3. The thermal conductivity of the SiNWs

On the basis of the series thermal-resistance model, we calculated the thermal conductivity of the SiNWs from equation (3) and performed the error propagation analysis represented by equation (4) as follows:

$$\frac{L_{SSCs}}{k_{SSCs}} = \frac{L_{SiNWs}}{k_{SiNWs}} + \frac{L_{SSCs} - L_{SiNWs}}{k_{Si}} \quad (3)$$

$$\Delta k_{SiNWs} = \left[\left(\frac{\partial k_{SiNWs}}{\partial k_{Si}}\Delta k_{Si}\right)^2 + \left(\frac{\partial k_{SiNWs}}{\partial k_{SSCs}}\Delta k_{SSCs}\right)^2 + \left(\frac{\partial k_{SiNWs}}{\partial L_{SiNWs}}\Delta L_{SiNWs}\right)^2 + \left(\frac{\partial k_{SiNWs}}{\partial L_{SSCs}}\Delta L_{SSCs}\right)^2\right]^{1/2}. \quad (4)$$

Here, L_{SSCs} and L_{SiNWs} indicate the lengths of the SSCs and SiNWs given in table 1. k_{SSCs}, k_{SiNWs} and k_{Si} represent the thermal conductivities of the SSCs, the SiNWs and the corresponding Si wafers. A Δ preceding a symbol denotes an error value. Because the sprayed graphite film is very thin and its thermal conductivity is much higher compared to that of the SSCs, the thermal resistances from the graphite films and the graphite–SiNW interface are small enough to neglect. The results presented in figure 5(b) indicate that the SiNWs show inferior thermal conductivities and that increasing the surface roughness or porosity can significantly reduce the thermal conductivity. Furthermore, the thermal conductivities of the porous SiNWs are lower than those of the rough SiNWs, which can be readily observed by comparing the thermal conductivities of the n-type SiNWs with those of the p-type SiNWs. For example, the P-SiNWs prepared with an etching time of 30 min, which have nanopores, display a thermal conductivity of 12.06 W m^{-1} K^{-1} at 300 K; this value is below that of the smooth N-SiNWs prepared with an etching time of 30 min (19.74 W m^{-1} K^{-1}) and close to that of the rough N-SiNWs prepared with an etching time of 120 min (13.50 W m^{-1} K^{-1}). Meanwhile, the thermal conductivity of the rough N-SiNWs that were etched for 240 min is 8.48 W m^{-1} K^{-1}, and the porous P-SiNWs that were etched for 240 min have a lower thermal conductivity

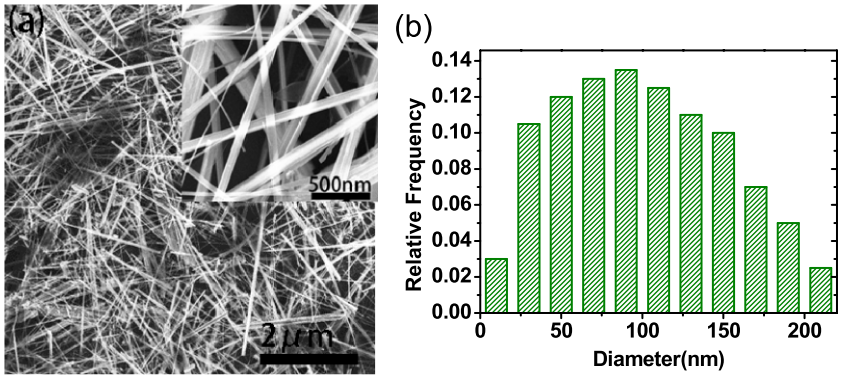

Figure A.1. (a) The SEM image of the silicon nanowires scraped off the silicon substrate. (b) The histogram of the different diameter wires in the silicon nanowire arrays.

of 1.68 W m^{-1} K^{-1} at 300 K, which is comparable to that of individual silicon nanowires with a 52 nm diameter [14]. From figure 5(b), we can also observe that the thermal conductivities of the SiNWs that were etched for 180 to 240 min are nearly identical as there is little difference in their morphologies, as seen in the previous analysis. This provides further evidence that the surface conditions of the SiNWs can remarkably impact upon their thermal conductivities. The significant reduction of the thermal conductivity in the SiNWs could be attributed to the size effect and the high specific surface area, resulting in strong phonon-boundary scattering. The phonon-boundary scattering would certainly be enhanced by the increased roughness of the silicon nanowire surface, especially for nanowires with diameters smaller than the bulk phonon mean free path. In porous SiNWs, the pore interface-phonon scattering contributes to a reduction in the thermal conductivity in addition to the phonon-boundary scattering. This is why porous SiNWs have lower thermal conductivities than rough SiNWs.

4. Conclusion

In summary, by adjusting the etching time and doped concentration, we have synthesized vertical SiNWs of 20–200 nm diameters with a variety of lengths, roughnesses and porosities on single-crystal silicon wafers with the metal-assisted chemical etching method. The results suggest that long and rough SiNWs would form on lightly doped wafers with longer etching times, while long and porous SiNWs would be obtained on highly doped wafers with longer etching times. We also found that the highly doped bulk silicon wafer has a lower thermal conductivity than the lightly doped wafer and that the thermal conductivities of the SSCs sharply decrease with increases in the length, surface roughness and porosity of the SiNWs. When the wafer is etched for 240 min, the thermal conductivity of the P-SSCs drops to 7.12 W m^{-1} K^{-1}, which is 11.44 times lower than that of a silicon wafer with the same dopant concentration at room temperature. Moreover, because of the combined effects of phonon-boundary and pore interface-phonon scattering, the thermal conductivities of porous SiNWs are lower than those of rough SiNWs, as only phonon-boundary scattering contributes in the latter case. What is particularly attractive is that etching porous SiNWs for 240 min can significantly reduce the thermal conductivity to as low as 1.68 W m^{-1} K^{-1} at 300 K, which is of the same magnitude as the thermal conductivity of an individual silicon nanowire reported previously. However, compared with an individual silicon nanowire and groups of such wires, large-scale SiNWs and SSCs would be more efficient and practical for application to enhance the performance of thermoelectric devices.

Acknowledgments

This work was supported by the National Basic Research Program of China (No. 2010CB832905), and partially supported by the Key Scientific and Technological Project of the Ministry of Education of China (No. 108124).

Appendix

To facilitate the statistics, we scraped the nanowires off the silicon substrate and measured randomly the diameters of 200 nanowires using the software of Image-Pro Plus and the SEM images (figure A.1(a)). Figure A.1(b) shows the histogram of the different diameter wires in the silicon nanowire arrays.

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